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08EC047

M.Tech. Degree Examination, December 2010
Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the need for low power VLSI design. **(04 Marks)**

b. A 32 bit off – chip bus operating at 5V and 66 MHz clock rate is driving capacitance of 25 pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus? **(04 Marks)**

c. Explain the basic principles of low power VLSI design. **(12 Marks)**

2 a. Explain the short circuit current of an inverter, with the help of a neat diagram. **(10 Marks)**

b. Discuss the impact of transistor sizing, gate oxide thickness and technology scaling on low power electronics, with suitable diagram. **(10 Marks)**

3 a. With a neat diagram, explain the dual bit type signal model for DSP system. Explain how data path module is characterized for the module, with one input and one output such as a FIFO queue, with relevant capacitance and power expressions. **(10 Marks)**

b. Discuss in brief about SPICE basics, SPICE power analysis. Also explain the discrete transistor modeling and analysis. **(10 Marks)**

4 a. Explain in brief the static probability and derive an expression for conditional probability and frequency. **(10 Marks)**

b. Briefly explain entropy and explain in detail how power estimation is done using entropy analysis of a combinational circuit. **(10 Marks)**

5 a. Mention different types of power consumption in CMOS circuits and discuss in detail about terms glitches, pre charged circuits and reduced voltage swing in CMOS circuits. **(10 Marks)**

b. With a neat circuit diagram, discuss the following flip – flops :
i) Static flip flop ; ii) Dynamic flip flop. **(10 Marks)**

6 a. Mention different transformation operators used in gate re-organization. **(04 Marks)**

b. Explain the concept of bus invert encoding, with relevant expression. **(08 Marks)**

c. Explain the basics of pre – computation logic, with a neat block schematic. **(08 Marks)**

7 a. Discuss the effects of voltage reduction on parallel architecture. **(10 Marks)**

b. Discuss the following low power full adder circuits with relevant circuit diagram :
i) NO RACE dynamic CMOS LOGIC (NORA) full adder.
ii) Cascade Voltage Switch Logic (CVSL) full order. **(10 Marks)**

8 a. Explain the concept of buffer insertion in an equal path length clock tree using :
i) Balanced buffer insertion ; ii) Level by level method. **(10 Marks)**

b. Describe the power minimization technique at algorithm level. **(10 Marks)**

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